Digilent Nexys LCD Module™ Reference Manual

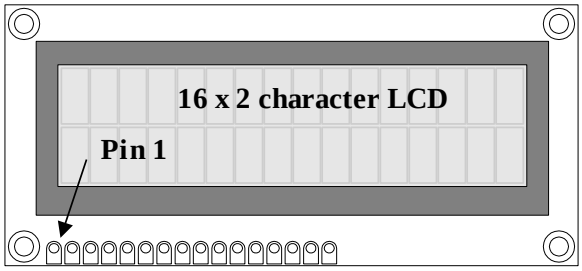
www.digilentinc.com

215 E Main Suite D | Pullman, WA 99163
(509) 334 6306 Voice and Fax

Revision: 7 Feb 2007

Overview

The Digilent NxLCD is a 16x2 character LCD module that includes a standard 16-pin parallel interface. Solder-length pins are preloaded into the connector, allowing it to plug directly into a Nexys or Spartan 3E-1600 board, or to easily attach to any other board via a standard 100-mil spaced connector.



Powertip PC1602ARS

The LCD display uses a standard character display controller (the ST7066Ufrom Sitronix, the HD44780 from multiple vendors, KS0066 from Samsung, and the SED1278 from Epson), so designs can take advantage of a large existing body of reference designs and materials.

Pin	Signal	Description
1	Vss	System GND
2	Vdd	System PWR (5VDC)
3	Vo	Contrast V (~300mV)
4	RS	Register Select
5	R/nW	Read '1' / Write '0'
6	E	Enable reads/writes
7	DB0	Data 0
8	DB1	Data 1
9	DB2	Data 2
10	DB3	Data 3
11	DB4	Data 4
12	DB5	Data 5
13	DB6	Data 6
14	DB7	Data 7
15	K	Backlight cathode (N/A)
16	A	Backlight anode (NA)

Functional Description

The DIO5 uses a Powertip 16x2 LCD module (P/N PC1602ARS-DWA-A) with a Samsung KS0066U controller (data sheets are available at the Digilent website).

The KS0066U contains a character-generator ROM (CGROM) with 208 preset 5x8 character patterns, a character-generator RAM (CGRAM) that can hold 8 user-defined 5x8 characters, and a display data RAM (DDRAM) that can hold 80 character codes. Character codes written into the DDRAM serve as indexes into the CGROM (or CGRAM). Writing a character code into a particular DDRAM location will cause the associated character to appear at the corresponding display location. Display positions can be shifted left or right by setting a bit in the instruction register (IR). The write-only IR directs display operations (such as clear display, shift left or right, set DDRAM address, etc). Available instructions (and the associated IR codes) are shown in the right-most column of table 3 below. A busy flag shows whether the display has competed the last requested operation; prior to initiating a new operation, the flag can be checked to see if the previous operation has been completed.

The display has more DDRAM locations than can be displayed at any given time. DDRAM locations 00H to 27H map to the first display row, and locations 40H to 67H map to the second row. Normally,

DDRAM location 00H maps to the upper left display corner, and 40H to the lower left. Shifting the display left or right can change this mapping. The display uses a temporary data register (DR) to hold data during DDRAM /CGRAM reads or writes, and an internal address register to select the RAM location. Address register contents, set via the IR, are automatically incremented after each read or write operation. The LCD display uses ASCII character codes. Codes up through 7F are standard ASCII (which includes all “normal” alphanumeric characters). Codes above 7F produce various international characters – please see the manufacturers data sheet for more information on international codes.

The display is connected to the DIO5 board by a 16-pin connector (pins 15 and 16 are for an optional backlight, and they are not used). The 14-pin interface includes eight data signals, three control signals, and three voltage supply signals. The eight data bus signals are passed through the CPLD to/from the system bus for read/write cycles directed to the LCD memory space (address 10X). The three LCD control signals are driven from the CPLD: the RS (Register Strobe) signal clocks data into registers; the R/W signal determines bus direction; and the E signal enables the bus for read or write operations. In the standard CPLD configuration, the R/S and R/W signals are connected to ADDR0 and WE respectively. The E signal can be driven directly from the LCDEN signal available on the system connector, or if LCDEN is left at logic ‘0’, then E is driven whenever address “10X” is present on the bus, CS is asserted, and AS or DS are low. LCD bus signals and timings are shown below.

A startup sequence with specific timings ensures proper LCD operation. After power-on, at least 20ms must elapse before the function-set instruction code can be written to set the bus width, number of lines, and character patterns (8-bit interface, 2 lines, and 5x8 dots are appropriate). After the function-set instruction, at least 37us must elapse before the display-control instruction can be written (to turn the display on, turn the cursor on or off, and set the cursor to blink or no blink). After another 37us, the display-clear instruction can be issued. After another 1.52ms, the entry-mode instruction can set address increment (or address decrement) mode, and display shift mode (on or off). After this sequence, data can be written into the DDRAM to cause information to appear on the display.

Table 3. LCD Instructions and Codes

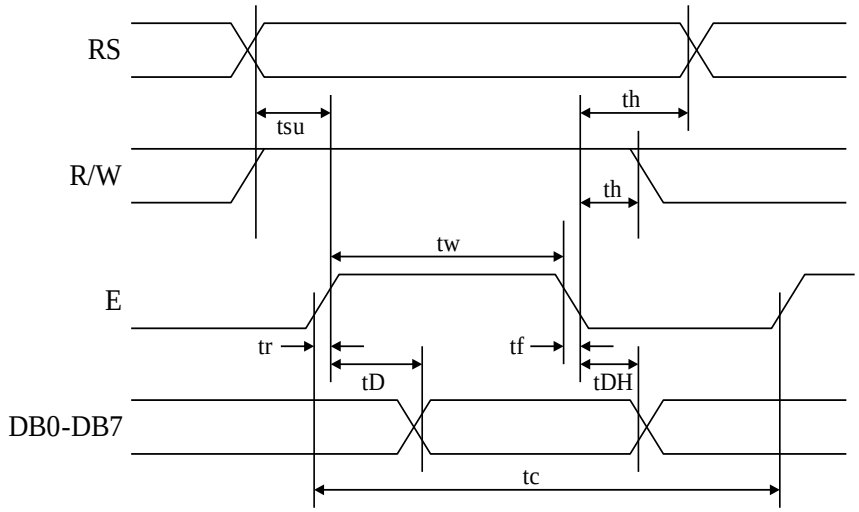
Instruction	Instruction bit assignments										Description
	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
Clear Display	0	0	0	0	0	0	0	0	0	1	Clear display by writing a 20H to all DDRAM locations; set DDRAM address register to 00H; and return cursor to home.
Return Home	0	0	0	0	0	0	0	0	1	X	Return cursor to home (upper left corner), and set DDRAM address to 0H. DDRAM contents not changed.
Entry mode set	0	0	0	0	0	0	0	1	I/D	SH	I/D = '1' for right-moving cursor and address increment; SH = '1' for display shift (direction set by I/D bit).
Display ON/OFF control	0	0	0	0	0	0	1	D	C	B	Set display (D), cursor (C), and blinking cursor (B) on or off.
Cursor or Display shift	0	0	0	0	0	1	S/C	R/L	X	X	SC = '0' to shift cursor right or left, '1' to shift entire display right or left (R/L = '1' for right).
Function Set	0	0	0	0	1	DL	N	F	X	X	Set interface data length (DL = '1' for 8 bit), number of display lines (N = '1' for 2 lines), display font (F = '0' for 5x 8 dots)
Set CGRAM Address	0	0	0	1	AC5	AC4	AC3	AC2	AC1	AC0	Set CGRAM address counter
Set DDRAM address	0	0	1	AC6	AC5	AC4	AC3	AC2	AC1	AC0	Set DDRAM address counter
Read busy flag/ address	0	1	BF	AC6	AC5	AC4	AC3	AC2	AC1	AC0	Read busy flag and address counter
Write data to RAM	1	0	D7	D6	D5	D4	D3	D2	D1	D0	Write data into DDRAM or CGRAM, depending on which address was last set
Read data from RAM	1	1	D7	D6	D5	D4	D3	D2	D1	D0	Read data from DDRAM or CGRAM, depending on which address was last set

Table 4. LCD Connector Signals

Pin No.	Symbol	Signal Description
1	Vss	Signal ground
2	Vdd	Power supply (5V)
3	Vo	Operating (contrast) voltage (LCD drive, typically 100mV at 20C)
4	RS	Register select: high for data transfer, low for instruction register
5	R/W	Read/write signal: high for read mode, low for write mode

6	E	Read/write strobe: high for read OE; falling edge writes data
7-14	Data Bus	Bi-directional data bus

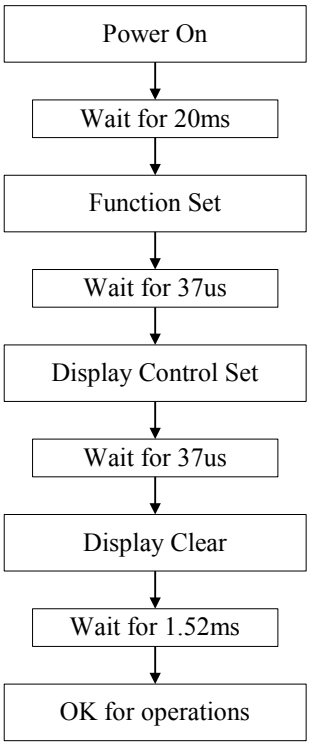
LCD Read Cycle



LCD Write Cycle

Table 5. LCD Bus Timings

Parameter	Symbol	Min	Max	Unit	Test Pin
Enable cycle time	tc	500		ns	E
Enable High pulse width	tw	220		ns	E
Enable rise/fall time	tr, tf		25	ns	E
RS, R/W setup time	tsu	40		ns	RS, R/W
RS, R/W hold time	th	10		ns	RS, R/W
Read data output delay	tD	60	120	ns	DB0-DB7
Read data hold time	tDH	20		ns	DB0-DB7
Write data setup time	tsu1	40		ns	DB0-DB7
Write data hold time	th1	10		ns	DB0-DB7



LCD startup sequence