EVB-USB3300-XLX User Manual

1 Introduction

The SMSC USB3300 USB Transceiver features a ULPI interface to support systems implementing a USB Host, Device, or On-the-Go (OTG) system. SMSC supplies a complete family of PHY products to meet the needs of many applications.

2 Overview

The EVB-USB3300-XLX is a Daughter Card designed to plug into a user's Xilinx ML401 development system using a header connector. The card attaches to a USB link layer to create a USB Host, Device, or On-the-Go (OTG) system. The digital interface meets the UTMI+ Low Pin Interface (ULPI) specification. The ULPI specification can be downloaded from the SMSC web site at http://www.smsc.com/main/catalog/usb3300.html. The EVB-USB3300-XLX includes the USB300 and all associated external components. Figure 3 shows a schematic of the EVB.

2.1 3.3 Volt Power Supply

The EVB-USB3300-XLX requires a 3.3 volt supply capable of providing 80mA of current to be present at the J2 header pins 16, 19, 22 and 25. For device only applications this is the only power the EVB-USB3300-XLX requires.

2.2 Crystal Oscillator

A 24 MHz crystal is connected to the internal oscillator of the USB3300. A PLL circuit in the USB3300 generates the 60MHz CLKOUT signal used by the link layer.

2.3 USB Connector

A standard Mini-AB connector is provided to attach a USB cable.

2.4 Supplying VBUS Power

In host or OTG applications the EVB-USB3300-XLX must provide 5 volts on V_{BUS}. The EVB-USB3300-XLX includes a 5 volt switch that can connect 5 volts to V_{BUS}. The EVB-USB3300-XLX 5 volt supply can come from either external power supplied at J5 or from header J1 pins 1, 4, 7 and 10. Jumper J6 must be installed to source +5V for the ML501 header. When using J5 to supply external power, J6 must be removed.

The 5 volt switch is controlled by the CPEN signal from the USB3300. The CPEN state is controlled by ULPI registers in the USB3300 per the ULPI specification. The 5 volt switch has an undervoltage lockout that turns the switch off if the VBUS voltage is low and the switch prevents reverse current flow (backdrive) when in the off state. The switch does not provide protection from reverse currents when in the on state. The user should take care to ensure the switch is off when V_{BUS} is being sourced by the USB cable.

In host mode, connector J7 should be installed to add capacitance to V_{BUS}. The USB2.0 specification requires this extra capacitance be present in host implementations.

2.5 Digital I/O

The ULPI signals are routed to connector J1 for connection to the ML401. Each signal on J1 is described in Table 2.1. All ULPI signals are 3.3V CMOS compatible.

Table 2.1 Signals on 3x13-Pin Header

J1 Pin	Signal Name	J1 Pin	Signal Name	J1 Pin	Signal Name
1	**+5V**	**2**	GND	**3**	Reset
4	**+5V**	**5**	GND	**6**	NXT
7	**+5V**	**8**	GND	**9**	CLKOUT
10	**+5V**	**11**	GND	**12**	DIR
13	**NC**	**14**	GND	**15**	STP
16	**+3.3V**	**17**	GND	**18**	DATA7
19	**+3.3V**	**20**	GND	**21**	DATA6
22	**+3.3V**	**23**	GND	**24**	DATA5
25	**+3.3V**	**26**	GND	**27**	DATA4
28	**NC**	**29**	GND	**30**	DATA3
31	**RSVD1**	**32**	GND	**33**	DATA2
34	**RSVD2**	**35**	GND	**36**	DATA1
37	**RSVD3**	**38**	GND	**39**	DATA0

2.6 ULPI Signal Test Points

The headers J2, J3 and J4 provide easy access to the ULPI signals, and each pin has a silk screen label as shown in Figure 1 .

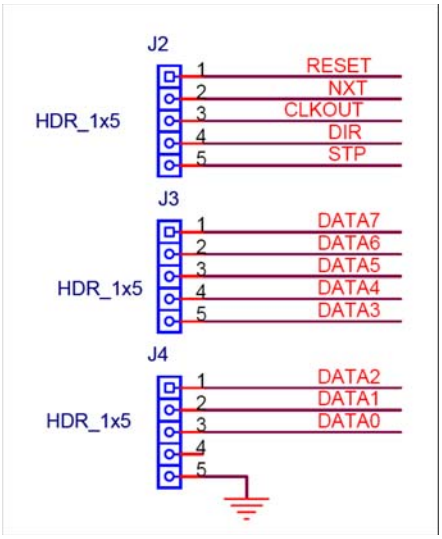

Figure 1 ULPI Signal Test Points

2.7 Block Diagram

The EVB-USB3300-XLX block diagram shows how the jumpers are used on the board.

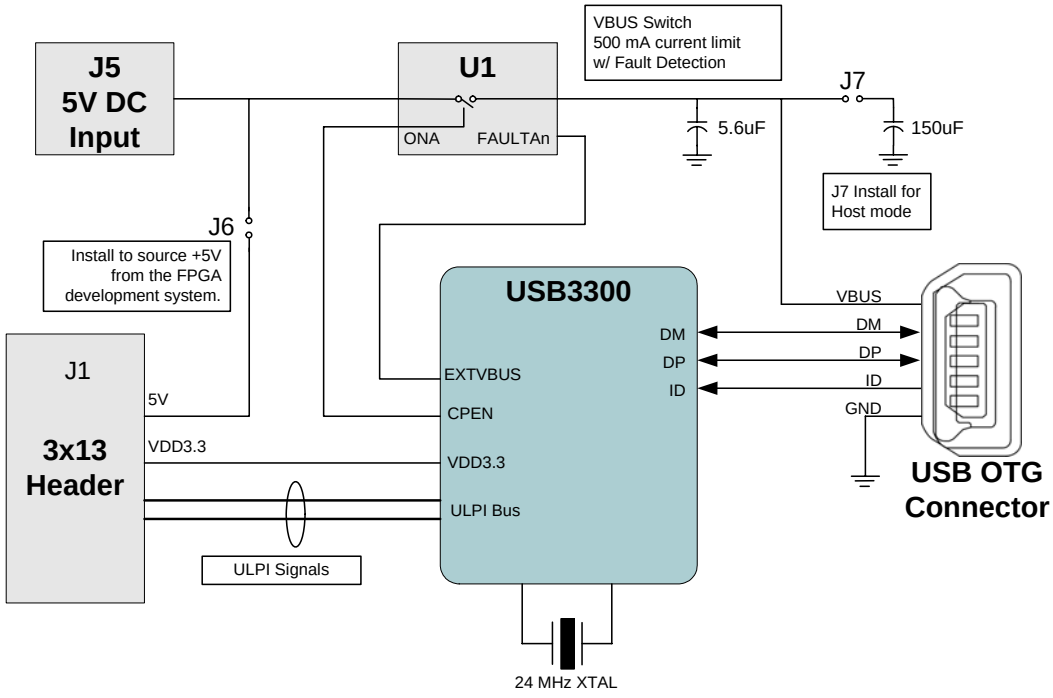

Figure 2 EVB-USB3300-XLX Block Diagram

2.8 Schematic Diagram

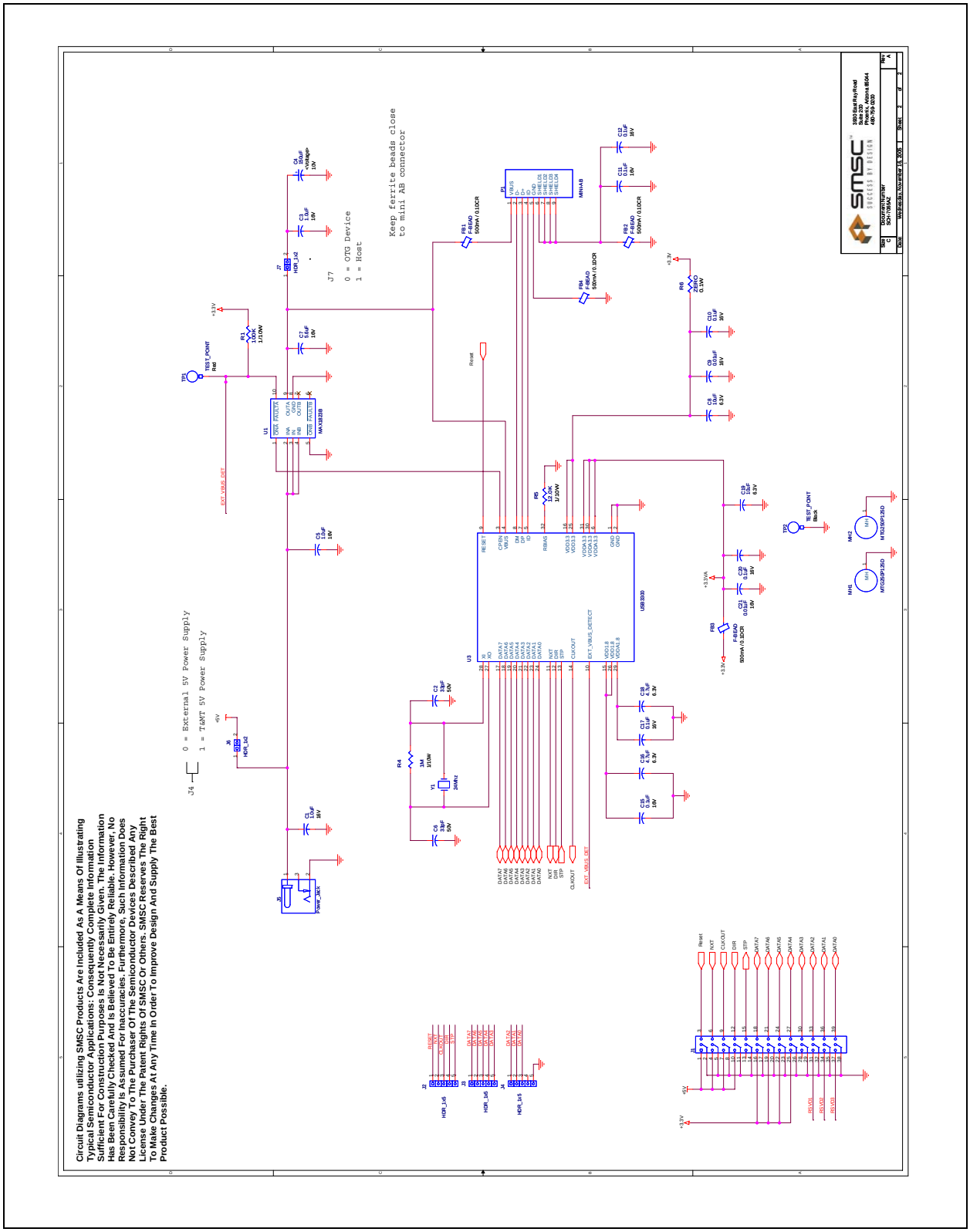

Figure 3 EVB-USB3300-XLX Schematic